Abstract of the Disclosure

Phase locked loops operable at low reference clock signal frequencies include a phase comparator having a phase detector, a digital counter, and a digital-to-analog converter. The phase detector provides an error signal indicative of a phase relationship between the reference clock signal and a feedback signal. The digital counter provides a count value indicative of the amount of phase error between the reference clock signal and the feedback signal. The digital-to-analog converter provides an error voltage signal proportional to the count value. Such phase comparators permit direct measurement of the amount of phase error prior to filtering and amplification by the phase locked loop. Direct measurement of the amount of phase error can be used to reduce the likelihood of saturating an amplifier of an active filter of the phase locked loop without the use of a pre-filter. Such phase locked loops are suitable for use in timing circuits of communications systems.